



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/754,416	01/09/2004	Yoshihiro Kawakita	10873.787USD1	7941
7590	05/03/2006		EXAMINER	
Hamre, Schumann, et al PO Box 2902-0902 Minneapolis, MN 55402			PHAN, THIEM D	
			ART UNIT	PAPER NUMBER
				3729

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

88

Office Action Summary	Application No.	Applicant(s)
	10/754,416	KAWAKITA ET AL.
	Examiner	Art Unit
	Tim Phan	3729

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 07 March 2006.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 12-46 is/are pending in the application.
- 4a) Of the above claim(s) 17-46 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 12-16 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>1/9/04</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

Election/Restrictions

1. Applicants' election without traverse of Species A, Claims 12-16, filed on 3/07/06, is acknowledged (correcting a typo in Species A for Claims 12-14 in applicants' response).

The Restriction mailed on 2/16/06 has been carefully reviewed and is held to be proper. Moreover Applicants did not distinctly and specifically point out any error in the Restriction Requirement. Accordingly, Claims 17-45 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species, there being no allowable generic or linking claim.

The Restriction filed on 2/16/06 is hereby made Final.

Applicants are required to cancel these nonelected claims (17-45) or take other appropriate action.

An Office Action on the merits of Claims 12-16 now follows.

Specification

2. The disclosure is objected to because of the following informalities:

- On page 1, before "ACKGROUND OF THE INVENTION", insert:

“CROSS REFERENCE TO RELATED DOCUMENTS:

This application is a Division of U.S. Application No. 09/956,205, filed on 9/18/01, US Patent No. 6,734,375, which claims the benefit of Japanese Patent Application No. 2000-282120, filed on 9/18/00.”;

- The following title is suggested: “Method of Manufacturing a Double-sided Circuit Board”.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakatani et al (US 5,484,647) in view of Fukutake et al (US 5,473,118).

With regard to claim 12, Nakatani et al teach a method for manufacturing a double side printed circuit board ((Fig. 1A-2D; col. 14, lines 20-24), comprising:

- providing a through hole (Fig. 1B, 103) in a laminate (Fig. 1B, 102) in which mold release films (Fig. 1B, 101) are formed on both surfaces of a circuit board electrically insulating material that is a circuit board electrically insulating sheet comprising a porous

sheet (Fig. 1B, 102a) in which an additional layer of Si-type lubricant (Col. 10, line 42) is laminated to at least one surface of the porous sheet and at least a central portion of the porous sheet is not completely impregnated with that extra material; except for having that extra layer as resin;

- filling the through hole with a conductive paste (fig. 1C, 104);
- peeling off the mold release film (Figs. 2A-2B, 101) from the laminate in which the through hole is filled with the conductive paste;
- superimposing metal foils (Fig. 2B, 105) on both surfaces of the circuit board electrically insulating material from which the mold release films have been peeled off to form a laminate;
- heating and pressing the laminate (Fig. 2C, 102) to allow the metal foils to be adhered to the porous sheet, and compressing and hardening the conductive paste filled in the through hole, thereby providing an inner via hole; and
- forming desired circuit patterns (Fig. 2D, 106) on the metal foil.

Fukutake et al teach a method of making printed circuit board (Figs. 1-4) with a porous sheet (Fig. 1, 3) in which a layer of resin (Fig. 1, 4; col. 4, lines 6-17) is laminated to at least one surface of the porous sheet and heating and pressing the laminate (Fig. 4, 3; col. 7, lines 1-5) to allow hollow pores of the porous sheet to be filled with resin, in order to restrain the adhesive from lateral flow and segregation (Col. 2, lines 1-23), and to have low dielectric constant PCB.

It would be obvious to one of ordinary skill in the art at the time the invention was made

to combine the two teachings by applying the resin layer to a porous sheet, as taught by Fukutake et al, to the method for manufacturing a double side printed circuit board, as taught by Nakatani et al, in order to restrain the adhesive from lateral flow and segregation, and to have low dielectric constant PCB.

With regard to claim 13, Nakatani et al and Fukutake et al teach a method of making printed circuit board including the migration of the resin into the pores of porous sheet by heat and pressure (Fukutake et al; Col. 5, lines 9-15), which reads on applicants' claimed invention, except for indicating that the pores size of the porous sheet, which absorbs the resin, to be smaller than the particle size of the conductive paste.

It would be obvious to one of ordinary skill in the art at the time the invention was made to realize that the pores size of the porous sheet must be smaller than the particle size of the conductive paste in order to absorb only the resin and to have low dielectric constant PCB.

With regard to claim 14, Nakatani et al and Fukutake et al teach a method of making printed circuit board including a conductive paste with conductive particles and resin (Nakatani et al; col. 5, lines 25+; col. 13, Table 1), wherein the conductive particles in the range 85 weight % and resin in the range from 10 weight %.

With regard to claim 15, Fukutake et al teach that the maximum hole diameter of the

pores of the porous sheet is 10 .mu.m or less (Col. 3, line 57).

With regard to claim 16, Nakatani et al teach that the porous sheet is a non-woven fabric containing a synthetic fiber as a main component (Col. 4, lines 60-64).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tim Phan whose telephone number is 571-272-4568. The examiner can normally be reached on M - F, 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Vo can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tim Phan
Examiner
Art Unit 3729

tp
April 28, 2006



A. DEXTER TUGBANG
PRIMARY EXAMINER